

04/04/2006 10/710826 Doty

L9 ANSWER 1 OF 24 CAPLUS COPYRIGHT 2006 ACS on STN

ACCESSION NUMBER: 2006:32926 CAPLUS

DOCUMENT NUMBER: 144:119457

TITLE: SOI semiconductor devices with two crystal orientations

INVENTOR(S): Kamata, Yoshiki; Nishiyama, Akira

PATENT ASSIGNEE(S): Toshiba Corp., Japan

SOURCE: Jpn. Kokai Tokkyo Koho, 17 pp.

CODEN: JKXXAF

DOCUMENT TYPE: Patent

LANGUAGE: Japanese

FAMILY ACC. NUM. COUNT: 1

PATENT INFORMATION:

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
JP 2006012995	A2	20060112	JP 2004-185389	20040623
PRIORITY APPLN. INFO.:			JP 2004-185389	20040623

AB The invention relates to a SOI semiconductor devices with two crystal orientations, wherein the second semiconductor layer is disposed on the first semiconductor layer via the insulating layer to accommodate two different types of devices.

IT 11148-21-3

RL: DEV (Device component use); USES (Uses)

(SOI semiconductor devices with two crystal orientations)

RN 11148-21-3 CAPLUS

CN Germanium alloy, nonbase, Ge,Si (9CI) (CA INDEX NAME)

Component Component
Registry Number

=====+=====

Ge 7440-56-4

Si 7440-21-3

CC 76-3 (Electric Phenomena)

ST crystal orientation SOI semiconductor device MISFET

MOSFET superlattice

IT Crystal orientation

MISFET (transistors).

MOSFET (transistors)

SOI devices

Semiconductor superlattices

(SOI semiconductor devices with two crystal orientations)

IT 7440-21-3, Silicon, uses 7440-56-4, Germanium, uses 7631-86-9, Silica, uses 11148-21-3

RL: DEV (Device component use); USES (Uses)

(SOI semiconductor devices with two crystal orientations)

04/04/2006 10/710826 Doty

L9 ANSWER 7 OF 24 CAPLUS COPYRIGHT 2006 ACS on STN

ACCESSION NUMBER: 2005:468614 CAPLUS

DOCUMENT NUMBER: 143:17805

TITLE: Strained silicon MOSFETs having improved thermal dissipation

INVENTOR(S): Pan, James N.; Goo, Jung-Suk; Xiang, Qi

PATENT ASSIGNEE(S): Advanced Micro Devices, Inc., USA

SOURCE: U.S., 17 pp.

CODEN: USXXAM

DOCUMENT TYPE: Patent

LANGUAGE: English

FAMILY ACC. NUM. COUNT: 1

PATENT INFORMATION:

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
-----	---	-----	-----	-----
US 6900143	B1	20050531	US 2003-658963	20030909
PRIORITY APPLN. INFO.:			US 2003-658963	20030909
AB	The thermal conductivity of strained silicon MOSFETs and strained silicon SOI MOSFETs is improved by providing a silicon germanium carbide thermal dissipation layer beneath a silicon germanium layer on which strained silicon is grown. The silicon germanium carbide thermal dissipation layer has a higher thermal conductivity than silicon germanium, thus providing more efficient removal of thermal energy generated in active regions.			
IC	ICM H01L021-461			
INCL	438752000; 257347000; 257348000; 257349000			
CC	76-3 (Electric Phenomena)			
ST	Strained silicon MOSFET silicon germanium carbide thermal dissipation			
IT	MOSFET (transistors)			
	SOI devices			
	Thermal conductivity			
	(strained silicon MOSFETs having improved thermal dissipation)			
IT	Semiconductor superlattices			
	(strained-layer; strained silicon MOSFETs having improved thermal dissipation)			
IT	79192-19-1			
	RL: DEV (Device component use); USES (Uses)			
	(strained silicon MOSFETs having improved thermal dissipation)			
REFERENCE COUNT:	4	THERE ARE 4 CITED REFERENCES AVAILABLE FOR THIS RECORD. ALL CITATIONS AVAILABLE IN THE RE FORMAT		

04/04/2006 10/710826 Doty

L9 ANSWER 13 OF 24 CAPLUS COPYRIGHT 2006 ACS on STN

ACCESSION NUMBER: 2005:238096 CAPLUS

DOCUMENT NUMBER: 142:289547

TITLE: Production method of a lattice relaxed single-crystal
SiGe layer for strained Si semiconductors

INVENTOR(S): Nakaharai, Makoto; Tezuka, Tsutomu

PATENT ASSIGNEE(S): Toshiba Corp., Japan

SOURCE: Jpn. Kokai Tokkyo Koho, 18 pp.

CODEN: JKXXAF

DOCUMENT TYPE: Patent

LANGUAGE: Japanese

FAMILY ACC. NUM. COUNT: 1

PATENT INFORMATION:

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
JP 2005072054	A2	20050317	JP 2003-209066	20030827
PRIORITY APPLN. INFO.:			JP 2003-209066	20030827

AB The invention relates to a production method of a lattice relaxed single crystal SiGe layer, suited for use in SOI-MOSFET containing a strained Si layer, wherein the annealing to melt only the high Ge containing layer in the two layers of SiGe, with different Ge concns., improves the lattice relaxation.

IT 11148-21-3

RL: DEV (Device component use); USES (Uses)

(production method of lattice relaxed single crystal SiGe layer for strained Si semiconductors)

RN 11148-21-3 CAPLUS

CN Germanium alloy, nonbase, Ge,Si (9CI) (CA INDEX NAME)

Component Component
Registry Number

=====+=====

Ge 7440-56-4

Si 7440-21-3

IC ICM H01L021-20

ICS H01L021-336; H01L027-12; H01L029-786

CC 76-3 (Electric Phenomena)

ST strained semiconductor silicon germanium lattice relaxation SOI MOSFET

IT MOSFET (transistors)

SOI devices

Structural relaxation

(production method of lattice relaxed single crystal SiGe layer for strained Si semiconductors)

IT Semiconductor superlattices

(strained layer; production method of lattice relaxed single crystal SiGe layer for strained Si semiconductors)

IT 11148-21-3

RL: DEV (Device component use); USES (Uses)

(production method of lattice relaxed single crystal SiGe layer for strained Si semiconductors)

04/04/2006 10/710826 . Doty

L9 ANSWER 14 OF 24 CAPLUS COPYRIGHT 2006 ACS on STN

ACCESSION NUMBER: 2005:181940 CAPLUS

DOCUMENT NUMBER: 142:271998

TITLE: Thin channel FET integrated circuit with recessed source/drains and extensions

INVENTOR(S): Chen, Huajie; Doris, Bruce B.; Oldiges, Philip J.; Wang, Xinlin; Zhu, Huilong

PATENT ASSIGNEE(S): International Business Machines Corporation, USA

SOURCE: U.S. Pat. Appl. Publ., 14 pp.

CODEN: USXXCO

DOCUMENT TYPE: Patent

LANGUAGE: English

FAMILY ACC. NUM. COUNT: 1

PATENT INFORMATION:

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
US 2005045947	A1	20050303	US 2003-604907	20030826
US 6924517	B2	20050802		
CN 1591899	A	20050309	CN 2004-10057601	20040820
PRIORITY APPLN. INFO.:			US 2003-604907	A 20030826

AB The invention relates to a **field effect** transistor (**FET**) integrated circuit (IC) chip. The devices have a thin channel, e.g., an ultra-thin (smaller than or equal to 10 nm (10 nm)) **silicon on insulator (SOI)** layer. Source/drain regions are located in recesses at either end of the thin channel and are substantially thicker (e.g., 30 nm) than the thin channel. Source/drain extensions and corresponding source/drain regions are self aligned to the **FET** gate and thin channel.

IT 11148-21-3
RL: DEV (Device component use); EPR (Engineering process); PEP (Physical, engineering or chemical process); PROC (Process); USES (Uses)
(**Si/SiGe superlattice SOI-structure field effect transistor integrated circuit**)

RN 11148-21-3 CAPLUS

CN Germanium alloy, nonbase, Ge, Si (9CI) (CA INDEX NAME)

Component	Component Registry Number
Ge	7440-56-4
Si	7440-21-3

IC ICM H01L029-76

ICS H01L029-745; H01L031-062

INCL 257336000; 257213000; 257333000

CC 76-3 (Electric Phenomena)

ST **SOI field effect transistor integrated circuit STI**

IT **Field effect transistors**

Integrated circuits

SOI devices

Superlattices

(**Si/SiGe superlattice SOI-structure**

field effect transistor integrated circuit)

IT 7440-21-3, Silicon, processes 7440-56-4, Germanium, processes

11148-21-3

RL: DEV (Device component use); EPR (Engineering process); PEP (Physical,

EIC 2800 MARY S. MIMS 272-5928

04/04/2006 10/710826 Doty

engineering or chemical process); PROC (Process); USES (Uses)
(Si/SiGe superlattice SOI-structure
field effect transistor integrated circuit).

04/04/2006 10/710826 Doty

L9 ANSWER 17 OF 24 CAPLUS COPYRIGHT 2006 ACS on STN

ACCESSION NUMBER: 2005:121257 CAPLUS

DOCUMENT NUMBER: 142:188848

TITLE: (Si-SiGe strained heterojunction CMOS)
transistor integrated circuit and fabrication thereof

INVENTOR(S): Ochimizu, Hirokato; Mishima, Yasuyoshi

PATENT ASSIGNEE(S): Fujitsu Limited, Japan

SOURCE: PCT Int. Appl., 74 pp.

CODEN: PIXXD2

DOCUMENT TYPE: Patent

LANGUAGE: Japanese

FAMILY ACC. NUM. COUNT: 1

PATENT INFORMATION:

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
WO 2005013375	A1	20050210	WO 2003-JP9885	20030805
W: CN, JP, US				
US 2006068557	A1	20060330	US 2005-272342	20051114
PRIORITY APPLN. INFO.:			(WO 2003-JP9885	A1 20030805

AB On an insulating layer formed on a silicon substrate, an NMOS transistor is formed in an NMOS transistor region and a PMOS transistor is formed in a PMOS transistor region. The NMOS transistor comprises a silicon layer, a silicon germanium layer in a lattice relaxed state formed on the silicon layer, a silicon layer in a tensilely strained state formed on the silicon germanium layer, and a gate electrode formed over the silicon layer with a gate insulating film interposed. The PMOS transistor comprises a silicon layer, a silicon germanium layer in a compressively strained state formed on the silicon layer, and a gate electrode formed over the silicon germanium layer with the gate insulating film interposed.

IT 11148-21-3
RL: DEV (Device component use); EPR (Engineering process); PEP (Physical, engineering or chemical process); PROC (Process); USES (Uses)
(Si-SiGe strained heterojunction CMOS transistor integrated circuit)

RN 11148-21-3 CAPLUS

CN Germanium alloy, nonbase, Ge,Si (9CI) (CA INDEX NAME)

Component Component
Registry Number

=====+=====

Ge 7440-56-4

Si 7440-21-3

IC ICM H01L029-786

ICS H01L021-336; H01L021-20; H01L021-8238; H01L027-092; H01L027-12

CC 76-3 (Electric Phenomena)

ST SOI CMOS transistor integrated circuit laser annealing etching

IT Etching

Ion bombardment

Laser annealing

MOS transistors

Semiconductor superlattices

(Si-SiGe strained heterojunction CMOS transistor integrated circuit)

EIC 2800 MARY S. MIMS 272-5928

04/04/2006 10/710826 Doty

IT 7440-21-3, Silicon, processes 11148-21-3

RL: DEV (Device component use); EPR (Engineering process); PEP (Physical, engineering or chemical process); PROC (Process); USES (Uses)

(Si-SiGe strained heterojunction CMOS transistor integrated circuit)

REFERENCE COUNT: 12 THERE ARE 12 CITED REFERENCES AVAILABLE FOR THIS RECORD. ALL CITATIONS AVAILABLE IN THE RE FORMAT

04/04/2006 10/710826 Doty

L9 ANSWER 19 OF 24 CAPLUS COPYRIGHT 2006 ACS on STN

ACCESSION NUMBER: 2004:1127015 CAPLUS

DOCUMENT NUMBER: 142:84452

TITLE: Fabrication of a SGOI wafer by annealing
near the alloy m.p.

INVENTOR(S): Bedell, Stephen W.; Chen, Huajie; Domenicucci, Anthony
G.; Fogel, Keith E.; Murphy, Richard J.; Sadana,
Devendra K.

PATENT ASSIGNEE(S): International Business Machines Corporation, USA

SOURCE: U.S. Pat. Appl. Publ., 22 pp., Cont.-in-part of U.S.
Ser. No. 448,948.

CODEN: USXXCO

DOCUMENT TYPE: Patent

LANGUAGE: English

FAMILY ACC. NUM. COUNT: 2

PATENT INFORMATION:

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
US 2004259334	A1	20041223	US 2004-855915	20040527
US 2004238885	A1	20041202	US 2003-448948	20030530
PRIORITY APPLN. INFO.:			US 2003-448948	A2 20030530

AB The invention relates to a process for making a low-defect, substantially relaxed SiGe-on-insulator substrate material. The method includes first forming a Ge-containing layer on a surface of a first single crystal Si layer which is present atop a barrier layer that is resistant to Ge diffusion. A heating step is then performed at a temperature that approaches the m.p. of the final SiGe alloy and retards the formation of stacking fault defects while retaining Ge. The heating step permits interdiffusion of Ge throughout the first single crystal Si layer and the Ge-containing layer thereby forming a substantially relaxed, single crystal SiGe layer atop the barrier layer. Moreover, because the heating step is carried out at a temperature that approaches the m.p. of the final SiGe alloy, defects that persist in the single crystal SiGe layer as a result of relaxation are efficiently annihilated therefrom. In one embodiment, the heating step includes an oxidation process that is performed at a temperature from about 1230° to about 1320°, for a time period of less than about 2 h. This embodiment provides SGOI substrate that have minimal surface pitting and reduced crosshatching.

IT 11148-21-3

RL: DEV (Device component use); EPR (Engineering process); PEP (Physical, engineering or chemical process); PROC (Process); USES (Uses)
(fabrication of SGOI wafer by annealing near the alloy m.p.)

RN 11148-21-3 CAPLUS

CN Germanium alloy, nonbase, Ge,Si (9CI) (CA INDEX NAME)

Component Component
Registry Number

=====+=====

Ge 7440-56-4

Si 7440-21-3

IC ICM H01L021-00

INCL 438478000

CC 76-3 (Electric Phenomena)

ST CMOS SIMOX CVD SGOI strained heterostructure

IT Vapor deposition process

EIC 2800 MARY S. MIMS 272-5928

04/04/2006 10/710826 Doty

(chemical; fabrication of SGOI wafer by annealing near the alloy m.p.)

IT Annealing

Heterojunction semiconductor devices

Ion implantation

Semiconductor **superlattices**)

(fabrication of SGOI wafer by annealing near the alloy m.p.)

IT 7440-21-3, Silicon, processes 7631-86-9, Silica, processes

11148-21-3

RL: DEV (Device component use); EPR (Engineering process); PEP (Physical, engineering or chemical process); PROC (Process); USES (Uses)

(fabrication of SGOI wafer by annealing near the alloy m.p.)

L9 ANSWER 23 OF 24 CAPLUS COPYRIGHT 2006 ACS on STN

ACCESSION NUMBER: 2001:389032 CAPLUS

DOCUMENT NUMBER: 135:13032

TITLE: Fabrication of semiconductor devices involving formation of thin SiGe layer on insulating layer and semiconductor devices having strained Si layer thereon

INVENTOR(S): Sugiyama, Naoharu; Mizuno, Tomohisa; Takagi, Shinichi; Kurobe, Atsushi

PATENT ASSIGNEE(S): Toshiba Corp., Japan

SOURCE: Jpn. Kokai Tokkyo Koho, 10 pp.

CODEN: JKXXAF

DOCUMENT TYPE: Patent

LANGUAGE: Japanese

FAMILY ACC. NUM. COUNT: 1

PATENT INFORMATION:

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
JP 2001148473	A2	20010529	JP 2000-270251	20000906
US 6326667	B1	20011204	US 2000-658191	20000908
			JP 1999-255154	A 19990909

PRIORITY APPLN. INFO.:

AB The process involves forming a strained SiGe layer on a substrate, injecting O ions, heating to form an oxide layer in the SiGe layer and to relax the lattice of the strained SiGe layer upon the oxide layer, and growing a strained Si layer on the lattice-relaxed SiGe layer. Preferably, a Si capping layer is formed on the strained SiGe layer to protect it in the heating process. On the lattice-relaxed SiGe may be formed a SiGe layer whereupon the strained Si layer will be formed. Before forming the strained Si layer, the surface of the lattice-relaxed SiGe layer may be etched. The surface of the lattice-relaxed SiGe layer may be treated with HF to form a H-terminated surface whereupon the strained Si layer will be formed. The H on the surface of the lattice-relaxed SiGe layer are preferably removed. After the oxidation process to form the oxide layer on the lattice-relaxed SiGe layer, the oxide layer may be removed by heating in vacuo, then the strained Si layer will be formed thereon. Preferably, on the substrate is formed a SiGe buffer layer whereupon the strained SiGe layer will be formed. Preferably, the substrate is Si or a SOI (silicon on insulator) type. The resulting semiconductor device comprises 1st SiGe layer on a substrate, an oxide layer on the 1st SiGe layer, ≤ 200 -nm thick 2nd SiGe layer lattice-relaxed and formed on the oxide layer, and a strained Si layer on the 2nd SiGe layer.

IT 59027-94-0, Germanium 0-20, silicon 80-100 (atomic)

RL: DEV (Device component use); USES (Uses)

(buffer; manufacture of semiconductor devices with insulating layer/thin SiGe/strained Si layer structure)

RN 59027-94-0 CAPLUS

CN Silicon alloy, base, Si 61-100, Ge 0-39 (9CI) (CA INDEX NAME)

Component	Component Percent	Component Registry Number
Si	61 - 100	7440-21-3
Ge	0 - 39	7440-56-4

04/04/2006 10/710826 Doty

IT 37380-03-3

RL: DEV (Device component use); USES (Uses)

(lattice-relaxed; manufacture of semiconductor devices with insulating layer/thin SiGe/strained Si layer structure)

RN 37380-03-3 CAPLUS

CN Silicon alloy, base, Si 61,Ge 39 (9CI) (CA INDEX NAME)

Component	Component Percent	Component Registry Number
Si	61	7440-21-3
Ge	39	7440-56-4

IT 12623-04-0 37232-85-2

RL: NUU (Other use, unclassified); USES (Uses)

(lattice-relaxed; manufacture of semiconductor devices with insulating layer/thin SiGe/strained Si layer structure)

RN 12623-04-0 CAPLUS

CN Germanium alloy, base, Ge 53,Si 47 (9CI) (CA INDEX NAME)

Component	Component Percent	Component Registry Number
Ge	53	7440-56-4
Si	47	7440-21-3

RN 37232-85-2 CAPLUS

CN Silicon alloy, base, Si 69,Ge 31 (9CI) (CA INDEX NAME)

Component	Component Percent	Component Registry Number
Si	69	7440-21-3
Ge	31	7440-56-4

IC ICM H01L027-12

ICS H01L021-205; H01L029-786

CC 76-3 (Electric Phenomena)

ST semiconductor device fabrication strained silicon layer; strained layer
superlattice semiconductor device fabrication; silicon
germanium underlayer formation semiconductor device; substrate
SOI semiconductor device strained silicon

IT MOSFET (transistors)

Semiconductor device fabrication

Semiconductor devices

(manufacture of semiconductor devices with insulating layer/thin SiGe/strained Si layer structure)

IT SOI devices

(manufacture of semiconductor devices with insulating layer/thin SiGe/strained Si layer structure on SOI substrates)

IT 59027-94-0, Germanium 0-20, silicon 80-100 (atomic)

RL: DEV (Device component use); USES (Uses)

(buffer; manufacture of semiconductor devices with insulating layer/thin SiGe/strained Si layer structure)

IT 116551-27-0, Silicon oxide (SiOx)

RL: DEV (Device component use); USES (Uses)

(buried oxide layer; manufacture of semiconductor devices with insulating layer/thin SiGe/strained Si layer structure)

IT 37380-03-3

04/04/2006 10/710826 Doty

RL: DEV (Device component use); USES (Uses)
(lattice-relaxed; manufacture of semiconductor devices with insulating
layer/thin SiGe/strained Si layer structure)

IT 12623-04-0 37232-85-2

RL: NUU (Other use, unclassified); USES (Uses)
(lattice-relaxed; manufacture of semiconductor devices with insulating
layer/thin SiGe/strained Si layer structure)

IT 7440-21-3, Silicon, uses

RL: DEV (Device component use); USES (Uses)
(strained; manufacture of semiconductor devices with insulating layer/thin
SiGe/strained Si layer structure)

04/04/2006 10/710826 Doty

L10 ANSWER 7 OF 27 CAPLUS COPYRIGHT 2006 ACS on STN

ACCESSION NUMBER: 2005:99736 CAPLUS

DOCUMENT NUMBER: 142:188807

TITLE: Deposition of SiGe on silicon-on-insulator structures and bulk substrates

INVENTOR(S): Bauer, Matthias

PATENT ASSIGNEE(S): Asm America, Inc., USA

SOURCE: PCT Int. Appl., 27 pp.

CODEN: PIXXD2

DOCUMENT TYPE: Patent

LANGUAGE: English

FAMILY ACC. NUM. COUNT: 1

PATENT INFORMATION:

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
WO 2005010946	A2	20050203	WO 2004-US23505	20040721
US 2005054175	A1	20050310	US 2004-897985	20040723
PRIORITY APPLN. INFO.:			US 2003-489691P	P 20030723

AB The invention relates to a process for making a SiGe-on-insulator structure strain-relaxed SiGe layer on a silicon wafer while minimizing defects. Amorphous SiGe layers are deposited by CVD from trisilane and GeH4. The amorphous SiGe layers are recrystd. over silicon by melt or solid phase epitaxy (SPE) processes. The melt processes preferably also cause diffusion of germanium to dilute the overall germanium content and essentially consume the silicon overlying the insulator. The SPE process can be conducted with or without diffusion of germanium into the underlying silicon, and so is applicable to SOI as well as conventional semiconductor substrates.

IT 11148-21-3

RL: DEV (Device component use); EPR (Engineering process); PEP (Physical, engineering or chemical process); PROC (Process); USES (Uses)

(CVD of SiGe on silicon-on-insulator structure and bulk substrate)

RN 11148-21-3 CAPLUS

CN Germanium alloy, nonbase, Ge,Si (9CI) (CA INDEX NAME)

Component Component
Registry Number

====+=====

Ge	7440-56-4
Si	7440-21-3

IC ICM H01L

CC 76-3 (Electric Phenomena)

ST CVD SPE SOI diffusion silicon germanium superlattice

IT Diffusion

SOI devices

Solid phase epitaxy

Superlattices

(CVD of SiGe on silicon-on-insulator structure and bulk substrate)

IT Vapor deposition process

(chemical; CVD of SiGe on silicon-on-insulator structure and bulk substrate)

EIC 2800 MARY S. MIMS 272-5928

04/04/2006 10/710826 Doty

IT 7440-21-3, Silicon, processes 7631-86-9, Silica, processes
11148-21-3

RL: DEV (Device component use); EPR (Engineering process); PEP (Physical,
engineering or chemical process); PROC (Process); USES (Uses)
(CVD of SiGe on silicon-on-insulator
structure and bulk substrate)

04/04/2006 10/710826 Doty

L10 ANSWER 17 OF 27 CAPLUS COPYRIGHT 2006 ACS on STN
ACCESSION NUMBER: 2002:941919 CAPLUS
DOCUMENT NUMBER: 138:245216
TITLE: Coupling anomalies in SimGen/Si/SiO2 waveguide systems
AUTHOR(S): Bieber, Amy E.; Brown, T. G.
CORPORATE SOURCE: Dept. Phys., Queensborough Community Coll., City Univ.
of New York, Bayside, NY, 11364, USA
SOURCE: Optics Express [online computer file] (2002), 10(20),
1139-1144
CODEN: OPEXFF; ISSN: 1094-4087
URL: http://www.opticsexpress.org/view_file.cfm?doc=%24%28%2C%3F%26K0%2D%20%0A&id=%24%28L%2B%2EK%20%2D%20%0A
PUBLISHER: Optical Society of America
DOCUMENT TYPE: Journal; (online computer file)
LANGUAGE: English
AB Sharp coupling anomalies exist in a **SiGe superlattice**
buried in a **Si-on-insulator** waveguide structure. The
authors study these anomalies using a rigorous coupled wave anal. and
examine their suitability for Si-compatible waveguide-mode-resonant
filters for optical telecommunications. Active functions could include
optical detection, switching, and modulation. The authors predict that a
very weak, sub band-edge absorption can improve filter contrast or provide
high quantum efficiency detection.
IT 11148-21-3
RL: DEV (Device component use); USES (Uses)
(coupling anomalies in SimGen/Si/SiO2 waveguide systems and their
application)
RN 11148-21-3 CAPLUS
CN Germanium alloy, nonbase, Ge,Si (9CI) (CA INDEX NAME)

Component	Component Registry Number
Ge	7440-56-4
Si	7440-21-3

CC 73-11 (Optical, Electron, and Mass Spectroscopy and Other Related
Properties)
IT Optical filters
Optical resonators
Optical waveguides
Superlattices
(coupling anomalies in SimGen/Si/SiO2 waveguide systems and their
application)
IT 7440-21-3, Silicon, uses 7631-86-9, Silica, uses 11148-21-3
RL: DEV (Device component use); USES (Uses)
(coupling anomalies in SimGen/Si/SiO2 waveguide systems and their
application)

REFERENCE COUNT: 13 THERE ARE 13 CITED REFERENCES AVAILABLE FOR THIS
RECORD. ALL CITATIONS AVAILABLE IN THE RE FORMAT

L10 ANSWER 15 OF 27 CAPLUS COPYRIGHT 2006 ACS on STN

ACCESSION NUMBER: 2003:200876 CAPLUS

DOCUMENT NUMBER: 138:246862

TITLE: Fabrication of a strained **superlattice**
SOI substrate for a transistor integrated
circuit

INVENTOR(S): Nozu, Kazuya; Sato, Nobuhiko

PATENT ASSIGNEE(S): Canon Inc., Japan

SOURCE: Jpn. Kokai Tokkyo Koho, 13 pp.

CODEN: JKXXAF

DOCUMENT TYPE: Patent

LANGUAGE: Japanese

FAMILY ACC. NUM. COUNT: 1

PATENT INFORMATION:

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
JP 2003078118	A2	20030314	JP 2001-264674	20010831
PRIORITY APPLN. INFO.:			JP 2001-264674	20010831

AB The invention relates to a process for making a semiconductor device,
i.e., a strained **superlattice** SOI substrate for a
transistor integrated circuit, comprising a **SiGe** multilayer
structure having low defect d.

IT **11148-21-3**
RL: DEV (Device component use); EPR (Engineering process); PEP (Physical,
engineering or chemical process); TEM (Technical or engineered material
use); PROC (Process); USES (Uses)
(fabrication of strained **superlattice** SOI substrate
for transistor integrated circuit)

RN **11148-21-3** CAPLUS

CN Germanium alloy, nonbase, Ge,Si (9CI) (CA INDEX NAME)

Component Component
Registry Number

=====+=====

Ge 7440-56-4

Si 7440-21-3

IC ICM H01L027-12

ICS H01L027-12; H01L021-336; H01L021-762; H01L029-786

CC 76-3 (Electric Phenomena)

ST germanium silicon strained **superlattice** SOI transistor
integrated circuit

IT Integrated circuits

SOI devices

Superlattices

Transistors

(fabrication of strained **superlattice** SOI substrate
for transistor integrated circuit)IT **11148-21-3**RL: DEV (Device component use); EPR (Engineering process); PEP (Physical,
engineering or chemical process); TEM (Technical or engineered material
use); PROC (Process); USES (Uses)(fabrication of strained **superlattice** SOI substrate
for transistor integrated circuit)

L10 ANSWER 16 OF 27 CAPLUS COPYRIGHT 2006 ACS on STN

ACCESSION NUMBER: 2003:200874 CAPLUS

DOCUMENT NUMBER: 138:246860

TITLE: (Fabrication of a strained **superlattice** SOI substrate for a transistor integrated circuit)

INVENTOR(S): Sato, Nobuhiko; Nozu, Kazuya

PATENT ASSIGNEE(S): Canon Inc., Japan

SOURCE: Jpn. Kokai Tokkyo Koho, 16 pp.

CODEN: JKXXAF

DOCUMENT TYPE: Patent

LANGUAGE: Japanese

FAMILY ACC. NUM. COUNT: 1

PATENT INFORMATION:

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
JP 2003078116	A2	20030314	JP 2001-264672	20010831
PRIORITY APPLN. INFO.:			JP 2001-264672	20010831

AB The invention relates to a process for making a semiconductor device, i.e., a strained **superlattice** SOI substrate for a transistor integrated circuit, comprising a SiGe multilayer structure having low defect d.

IT 11148-21-3
 RL: DEV (Device component use); EPR (Engineering process); PEP (Physical, engineering or chemical process); TEM (Technical or engineered material use); PROC (Process); USES (Uses)
 (fabrication of strained **superlattice** SOI substrate for transistor integrated circuit)

RN 11148-21-3 CAPLUS

CN Germanium alloy, nonbase, Ge,Si (9CI) (CA INDEX NAME)

Component Component
 Registry Number

=====+=====

Ge 7440-56-4

Si 7440-21-3

IC ICM H01L027-12
 ICS H01L027-12; H01L021-336; H01L021-762; H01L029-786

CC 76-3 (Electric Phenomena)

ST germanium silicon strained **superlattice** SOI transistor integrated circuit

IT Integrated circuits

SOI devices

Superlattices

Transistors

(fabrication of strained **superlattice** SOI substrate for transistor integrated circuit)

IT 11148-21-3

RL: DEV (Device component use); EPR (Engineering process); PEP (Physical, engineering or chemical process); TEM (Technical or engineered material use); PROC (Process); USES (Uses)

(fabrication of strained **superlattice** SOI substrate for transistor integrated circuit)

04/04/2006 10/710826 Doty

RECORD. ALL CITATIONS AVAILABLE IN THE RE FORMAT

L10 ANSWER 19 OF 27 CAPLUS COPYRIGHT 2006 ACS on STN

ACCESSION NUMBER: 2000:186936 CAPLUS

DOCUMENT NUMBER: 132:228757

TITLE: Si-based light-emitting materials

AUTHOR(S): Hamilton, B.

CORPORATE SOURCE: Department of Physics, University of Manchester,
Manchester, M601 QD, UK

SOURCE: Proceedings of the International School of Physics
"Enrico Fermi" (1999), Volume Date 1998,
141st(Silicon-Based Microphotonics: From Basics to
Applications), 21-46
CODEN: PIPFA7; ISSN: 0074-784X

PUBLISHER: IOS Press

DOCUMENT TYPE: Journal; General Review

LANGUAGE: English

AB The optical and electronic properties of different Si are reviewed with 36
refs. The light emission from macroscopic Si, electron-hole localization,
and selection rules are discussed. The optical properties were studied
for porous Si and Si nanoparticles and clusters. Energy transfer for
electroluminescence and Si-insulator multi quantum
well and superlattice structures are examined The SiGe
technol. is also mentioned.

CC 73-0 (Optical, Electron, and Mass Spectroscopy and Other Related
Properties)

Section cross-reference(s): 76

REFERENCE COUNT: 37 THERE ARE 37 CITED REFERENCES AVAILABLE FOR THIS
RECORD. ALL CITATIONS AVAILABLE IN THE RE FORMAT

04/04/2006 10/710826 Doty

L14 ANSWER 9 OF 13 WPIX COPYRIGHT 2006 THE THOMSON CORP on STN
ACCESSION NUMBER: 2002-617570 [66] WPIX
CROSS REFERENCE: 2005-201249 [21]
DOC. NO. NON-CPI: N2002-488764
DOC. NO. CPI: C2002-174520
TITLE: Photodetector for e.g., telecommunication systems, has
two separated silicide regions, and waveguide of
silicon-based material.
DERWENT CLASS: L03 U11 U12 V07
INVENTOR(S): JANZ, S; XU, D
PATENT ASSIGNEE(S): (CANA) NAT RES COUNCIL CANADA; (JANZ-I) JANZ S; (XUDD-I)
XU D
COUNTRY COUNT: 2
PATENT INFORMATION:

PATENT NO	KIND	DATE	WEEK	LA	PG	MAIN	IPC
US 2002079427	A1	20020627	(200266)*		10	H01L031-00	
CA 2365499	A1	20020626	(200266)	EN		H01L031-0256	
US 6815245	B2	20041109	(200474)			H01L021-00	

PRIORITY APPLN. INFO: US 2000-257285P 20001226; US
2001-21081 20011219

INT. PATENT CLASSIF.:
MAIN: H01L021-00; H01L031-00; H01L031-0256

BASIC ABSTRACT:

US2002079427 A UPAB: 20050401

NOVELTY - A photodetector comprises two separated silicide regions on a substrate; and a waveguide of a silicon-based material formed between sidewalls of the two separated silicide regions.

DETAILED DESCRIPTION - An INDEPENDENT CLAIM is included for a method of producing the photodetector having a waveguide of a silicon-based material, comprising depositing a metal layer on a silicon-based material layer of the substrate; etching to selectively remove unwanted regions of the metal layer; and heating the metal layer to induce a metal-silicon reaction to produce at least two separated silicide regions forming the waveguide of silicon-based material in between.

USE - For telecommunications systems, high capacity local area networks, and instrumentation.

ADVANTAGE - The photodetector is relatively simple, and has high quantum efficiency and fast response.

DESCRIPTION OF DRAWING(S) - The figure is a top view of a silicon-based photodetector with silicide waveguides.

Silicide regions 4

Silicon-based material layer 5

Dwg.1c/6

TECHNOLOGY FOCUS:

US 2002079427 A1UPTX: 20021014

TECHNOLOGY FOCUS - ELECTRONICS - Preferred Component: The two separated silicide regions (4) serve as electrodes. They are produced using a metal which is nickel, platinum, tungsten or cobalt. The photodetector has a tapered input waveguide. The substrate is a **silicon-on-insulator (SOI)** substrate.

Preferred Material: The silicon-based material is silicon, amorphous silicon, **silicon germanium** and/or amorphous **silicon germanium**. The silicon-based material layer (5) is made of silicon and epitaxially grown **silicon**

04/04/2006 10/710826 Doty

germanium superlattices, or silicon
germanium alloy and a silicon layer.

FILE SEGMENT: CPI EPI

FIELD AVAILABILITY: AB; GI

MANUAL CODES: CPI: L04-E05

EPI: U11-C18B4; U12-A02; V07-F01A1

04/04/2006 10/710826 Doty

L14 ANSWER 12 OF 13 WPIX COPYRIGHT 2006 THE THOMSON CORP on STN
ACCESSION NUMBER: 2001-032393 [05] WPIX
DOC. NO. NON-CPI: N2001-025321
DOC. NO. CPI: C2001-010016
TITLE: Method of manufacturing a photonic device e.g.,
photodetector involves alternately growing undulating
quantum well forming layers in a three dimensional growth
mode and barrier layers on a substrate.
DERWENT CLASS: L03 U11 U12
INVENTOR(S): JANZ, S; LAFONTAINE, H; XU, D X; XU, D
PATENT ASSIGNEE(S): (CANA) NAT RES COUNCIL CANADA
COUNTRY COUNT: 1
PATENT INFORMATION:

PATENT NO	KIND	DATE	WEEK	LA	PG	MAIN	IPC
CA 2271369	A1	20001107	(200105)*	EN	18	H01L031-00	
CA 2271369	C	20050301	(200517)	EN		H01L031-00	

PRIORITY APPLN. INFO: CA 1999-2271369 19990507
INT. PATENT CLASSIF.:

MAIN: H01L031-00

SECONDARY: C30B025-02; H01L031-0352

BASIC ABSTRACT:

CA 2271369 A UPAB: 20010124

NOVELTY - Photonic device manufacture involves forming a quantum well structure (4) on a substrate (1) by alternately growing a set of undulating quantum well forming layers and barrier layers on a substrate. The undulating quantum well forming layers are grown in a three dimensional growth mode to defeat the limitations imposed by strain on the maximum layer thickness.

DETAILED DESCRIPTION - An INDEPENDENT CLAIM is also included for a photonic device.

USE - The method is used for forming a photonic device e.g., photodetector (claimed).

ADVANTAGE - The photonic device has enhanced photoresponse at longer wavelengths, in particular 1550 nm, on a silicon substrate.

DESCRIPTION OF DRAWING(S) - The diagram shows a perspective view of an undulating waveguide photodetector grown on a **silicon** on **insulator** substrate.

Substrate 1

Buried oxide 2

Silicon buffer layer 3

Silicon germanium multiple quantum well
superlattice structure 4

Extension 5

Contact pads 6

Rectangular waveguide structure 7

Silicon layer 8

Dwg.1/6

TECHNOLOGY FOCUS:

CA 2271369 A1 UPTX: 20010124

TECHNOLOGY FOCUS - ELECTRONICS - Preferred Method: The undulating layers are formed with coherent wave thickness modulations. The layer thicknesses are selected so that the device has a photoresponse at 1550 nm. The quantum well structure is part of a waveguide structure formed on the

04/04/2006 10/710826 Doty

substrate.

TECHNOLOGY FOCUS - INORGANIC CHEMISTRY - Preferred Materials: The substrate is silicon. The quantum well forming layers consist of material of formula (I) and the barrier layers consist of silicon.
x approximately 0.5

Preferred Method: The quantum well forming layers are grown by ultrahigh vacuum chemical vapor deposition. The layers are formed by epitaxial growth. The waveguide structure is formed by etching the layers.

FILE SEGMENT: CPI EPI

FIELD AVAILABILITY: AB; GI

MANUAL CODES: CPI: L04-C01; L04-E05

EPI: U11-C01J4A; U11-C01J6; U11-C18B4; U12-A02B2A;
U12-A02B5D

04/04/2006 10/710826 Doty

L10 ANSWER 13 OF 27 CAPLUS COPYRIGHT 2006 ACS on STN

ACCESSION NUMBER: 2003:621625 CAPLUS

DOCUMENT NUMBER: 140:244062

TITLE: In-plane thermoelectric properties of Si/
Ge superlattice

AUTHOR(S): Liu, W. L.; Borca-Tasciuc, T.; Liu, J. L.; Taka, K.;
Wang, K. L.; Dresselhaus, M. S.; Chen, G.

CORPORATE SOURCE: Mechanical and Aerospace Engineering Department,
University of California at Los Angeles, CA, 90095,
USA

SOURCE: International Conference on Thermoelectrics (2001),
20th, 340-343

CODEN: ICTNBZ; ISSN: 1094-2734

PUBLISHER: Institute of Electrical and Electronics Engineers

DOCUMENT TYPE: Journal

LANGUAGE: English

AB In this paper we report exptl. investigation of the in-plane thermoelec.
properties of Si/Ge superlattices grown on
silicon-on-insulator wafers. A two-wire 3w method
was employed to measure the in-plane thermal conductivity of the
superlattice sample investigated. The in-plane Seebeck coefficient and
elec. conductivity of the same sample are also measured. Exptl. data are
compared with the results of theor. models of carrier transport based on
carrier pocket engineering and partial diffuse phonon interface
scattering.

IT 11148-21-3

RL: PRP (Properties); TEM (Technical or engineered material use); USES
(Uses)

(in-plane thermoelec. properties of Si/Ge
superlattice)

RN 11148-21-3 CAPLUS

CN Germanium alloy, nonbase, Ge,Si (9CI) (CA INDEX NAME)

Component Component
Registry Number

=====+=====

Ge 7440-56-4

Si 7440-21-3

CC 76-2 (Electric Phenomena)

Section cross-reference(s): 56

ST silicon germanium superlattice thermoelec
property

IT Electric conductivity

Seebeck effect

Semiconductor superlattices

Solid-solid interface

Thermal conductivity

(in-plane thermoelec. properties of Si/Ge
superlattice)

IT 11148-21-3

RL: PRP (Properties); TEM (Technical or engineered material use); USES
(Uses)

(in-plane thermoelec. properties of Si/Ge
superlattice)

REFERENCE COUNT: 12 THERE ARE 12 CITED REFERENCES AVAILABLE FOR THIS
RECORD. ALL CITATIONS AVAILABLE IN THE RE FORMAT

EIC 2800 MARY S. MIMS 272-5928

L10 ANSWER 18 OF 27 CAPLUS COPYRIGHT 2006 ACS on STN

ACCESSION NUMBER: 2000:661090 CAPLUS

DOCUMENT NUMBER: 133:301864

TITLE: Thermal conductivity of symmetrically strained **Si/Ge superlattices**

AUTHOR(S): Borca-Tasciuc, Theodorian; Liu, Weili; Liu, Jianlin; Zeng, Taofang; Song, David W.; Moore, Caroline D.; Chen, Gang; Wang, Kang L.; Goorsky, Mark S.; Radetic, Tamara; Gronsky, Ronald; Koga, Takaaki; Dresselhaus, Mildred S.

CORPORATE SOURCE: Mechanical and Aerospace Engineering Department, University of California, Los Angeles, CA, 90095-1597, USA

SOURCE: Superlattices and Microstructures (2000), 28(3), 199-206

CODEN: SUMIEK; ISSN: 0749-6036

PUBLISHER: Academic Press

DOCUMENT TYPE: Journal

LANGUAGE: English

AB Temperature-dependent thermal conductivity measurements in the cross-plane direction of sym. strained **Si/Ge superlattices**, and the effect of doping, period thickness and dislocations on the thermal conductivity reduction of **Si/Ge superlattices** are reported.

The **Si/Ge superlattices** are grown by mol.

beam epitaxy on **silicon** and **silicon-on-**

insulator substrates with a graded buffer layer. A differential

3 ω method is used to measure the thermal conductivity of the buffer and the

superlattices between 80 and 300 K. The thermal conductivity measurement

is carried out in conjunction with X-ray and TEM sample characterization.

The measured thermal conductivity values of the **superlattices** are lower than those of their equivalent composition bulk alloys. (c) 2000 Academic Press.

CC 69-5 (Thermodynamics, Thermochemistry, and Thermal Properties)

ST thermal cond sym strained **silicon germanium**

superlattice; doping thermal cond **silicon**

germanium superlattice; period thickness thermal cond

silicon germanium superlattice; dislocation

thermal cond **silicon germanium superlattice**

IT Semiconductor **superlattices**

Thermal conductivity

(thermal conductivity of sym. strained **Si/Ge superlattices**)

IT Crystal dislocations

Doping

(thermal conductivity of sym. strained **Si/Ge superlattices** in relation to)

IT Thickness

(thermal conductivity of sym. strained **Si/Ge superlattices** in relation to period thickness)

IT 7440-21-3, Silicon, properties 7440-56-4, Germanium, properties

RL: PRP (Properties)

(thermal conductivity of sym. strained **Si/Ge superlattices**)

IT 7440-36-0, Antimony, uses 7440-42-8, Boron, uses

RL: MOA (Modifier or additive use); USES (Uses)

(thermal conductivity of sym. strained **Si/Ge superlattices** doped with)

REFERENCE COUNT: 28 THERE ARE 28 CITED REFERENCES AVAILABLE FOR THIS RECORD. ALL CITATIONS AVAILABLE IN THE RE FORMAT

04/05/2006 10/710826 Doty

=> d his full

(FILE 'HOME' ENTERED AT 15:00:56 ON 04 APR 2006)

FILE 'CAPLUS' ENTERED AT 15:01:29 ON 04 APR 2006

FILE 'REGISTRY' ENTERED AT 15:01:33 ON 04 APR 2006

L1 734 SEA ABB=ON PLU=ON GE.SI/MF
L2 46 SEA ABB=ON PLU=ON GE SI/ELF

FILE 'CAPLUS' ENTERED AT 15:03:48 ON 04 APR 2006

L3 33181 SEA ABB=ON PLU=ON SIGE OR (SI OR SILICON) (2W) (GERMANIUM OR
GE)
L4 38075 SEA ABB=ON PLU=ON L1 OR L2 OR L3
L5 33318 SEA ABB=ON PLU=ON SUPERLATTICE OR SUPER(W)LATTICE OR
(DIGITAL OR MULTILAYER OR MULTI(W)LAYER) (2W)ALLO?
L6 26218 SEA ABB=ON PLU=ON SOS OR SOI OR (SI OR SIGE OR SILICON) (3W) (S
APPHIRE OR INSULATOR) OR SGOI
L7 51 SEA ABB=ON PLU=ON L4 AND L5 AND L6
L8 1540258 SEA ABB=ON PLU=ON MOSFET OR MOS OR FET OR MOS? OR PMOS? OR
NMOS? OR CMOS? OR METAL(W)OXIDE(2W)SEMICONDUCT? OR FIELD(W)EFFE
CT
L9 24 SEA ABB=ON PLU=ON L7 AND L8
D IBIB ABS HITSTR 1-24

FILE 'STNGUIDE' ENTERED AT 15:11:53 ON 04 APR 2006

FILE 'CAPLUS' ENTERED AT 15:19:40 ON 04 APR 2006

D L9 1-24 IBIB ABS HITSTR HITIND
L10 27 SEA ABB=ON PLU=ON L7 NOT L9
D IBIB ABS HITSTR HITIND
D IBIB ABS HITSTR HITIND 1-27

FILE 'CAPLUS' ENTERED AT 16:14:05 ON 04 APR 2006

FILE 'WPIX' ENTERED AT 16:32:28 ON 04 APR 2006

L11 11747 SEA ABB=ON PLU=ON SIGE OR (SI OR SILICON) (2W) (GERMANIUM OR
GE)
L12 3606 SEA ABB=ON PLU=ON SUPERLATTICE OR SUPER(W)LATTICE OR
(DIGITAL OR MULTILAYER OR MULTI(W)LAYER) (2W)ALLO?
L13 9204 SEA ABB=ON PLU=ON SOS OR SOI OR (SI OR SIGE OR SILICON) (3W) (S
APPHIRE OR INSULATOR) OR SGOI
L14 13 SEA ABB=ON PLU=ON L11 AND L12 AND L13
D IFULL 1-13

FILE 'JAPIO, COMPENDEX, KOREAPAT' ENTERED AT 16:46:11 ON 04 APR 2006

L15 15116 SEA ABB=ON PLU=ON L3
L16 19231 SEA ABB=ON PLU=ON L5
L17 18286 SEA ABB=ON PLU=ON L6
L18 13 SEA ABB=ON PLU=ON L15 AND L16 AND L17
L19 13 DUP REM L18 (0 DUPLICATES REMOVED)
D IALL 1-13

FILE 'INSPEC' ENTERED AT 16:52:48 ON 04 APR 2006

L20 2225 SEA ABB=ON PLU=ON (SI EL(S)GE EL(S)SI INT)/CHI
L21 2797 SEA ABB=ON PLU=ON (SI EL(S)GE EL)/CHI

EIC 2800 MARY S. MIMS 272-5928

Q4/05/2006 10/710826 Doty

L22 12867 SEA ABB=ON PLU=ON (SI BIN(S)GE BIN)/CHI
L23 20701 SEA ABB=ON PLU=ON SIGE OR (SI OR SILICON) (2W) (GERMANIUM OR
GE)
L24 23589 SEA ABB=ON PLU=ON L20 OR L21 OR L22 OR L23
L25 35244 SEA ABB=ON PLU=ON SUPERLATTICE OR SUPER(W)LATTICE OR
(DIGITAL OR MULTILAYER OR MULTI(W)LAYER) (2W)ALLO?
L26 16879 SEA ABB=ON PLU=ON SOS OR SOI OR (SI OR SIGE OR SILICON) (3W) (S
APPHIRE OR INSULATOR) OR SGOI
L27 20 SEA ABB=ON PLU=ON L24 AND L25 AND L26
D IALL 1-20

FILE 'JAPIO, COMPENDEX, INSPEC' ENTERED AT 17:06:27 ON 04 APR 2006
L28 33 DUP IDENTIFY L19 L27 (INCLUDES 5 SETS OF DUPLICATES)
D L28 TI 1-33

FILE 'CAPLUS' ENTERED AT 17:34:22 ON 04 APR 2006

L29 49 SEA ABB=ON PLU=ON "CHURCHILL A C"/AU
L30 18 SEA ABB=ON PLU=ON L3 AND L29
D 1-18 TI

L31 4 SEA ABB=ON PLU=ON L30 AND L5
D IBIB ABS HITIND 1-4
L32 0 SEA ABB=ON PLU=ON L30 AND L6

FILE 'SCISEARCH' ENTERED AT 17:44:41 ON 04 APR 2006

FILE 'CAPLUS' ENTERED AT 17:45:05 ON 04 APR 2006
L33 TRA L30 16 CIT : 1 TERM

FILE 'SCISEARCH' ENTERED AT 17:45:48 ON 04 APR 2006
L34 5 SEA ABB=ON PLU=ON L33
D TI 1-5
D 2,3,5 IBIB ABS
D 2,3,5 IALL